WHAT IS CLAIMED IS:

1. A non-volatile semiconductor memory device comprising:

a plurality of non-volatile semiconductor memory cells;

an interface making data exchange with an external device to write/read data with respect to the non-volatile semiconductor memory cells; and

a control circuit for controlling the non-volatile semiconductor memory cells,

wherein the interface and the control circuit include a first read mode booted via a first bootstrap to read data from the non-volatile semiconductor memory cells for continuously outputting (N + M)-byte (N is the n-th power of 2, n is positive integers) data via the interface, and a second read mode booted via a second bootstrap to read data from the non-volatile semiconductor memory cells for continuously outputting K-byte (K is the k-th power of 2, k is positive integers) data via the interface.

2. A non-volatile semiconductor memory device comprising:

a plurality of non-volatile semiconductor memory cells;

an interface making data exchange with an external device to write/read data with respect to the non-volatile semiconductor memory cells; and

a control circuit for controlling the non-volatile semiconductor memory cells,

wherein the interface and the control circuit include a first read mode booted via a first bootstrap to read data from the non-volatile semiconductor memory cells for continuously outputting (N + M)-byte (N is the n-th power of 2, n is positive integers, N > M) data via the interface, and a second read mode booted via a second bootstrap to read data from the non-volatile semiconductor memory cells for continuously outputting K-byte (K is the k-th power of 2, k is positive integers) data via the interface.

3. The device according to claim 1, wherein the first read mode is automatically transferred to output standby state after continuously outputting the data, and the second read mode is automatically transferred to a normal operation mode after continuously outputting the data.

4. The device according to claim 1, wherein the plurality of non-volatile semiconductor memory cells include ROM area storing system boot programs and area except for the ROM area, and in the second read mode, K (K > N) byte data is read from the ROM area.

5. The device according to claim 1, wherein the second read mode is booted according to a hardware reset signal supplied from an external device.

6. The device according to claim 1, wherein the

second read mode is booted based on a software reset command supplied from an external device.

7. The device according to claim 1, wherein during the second read mode, part of signals inputted to the interface is invalidated.

8. A non-volatile semiconductor memory device comprising:

a plurality of electrically data rewritable non-volatile semiconductor memory cells;

an interface making data exchange with an external device to read/write data with respect to the non-volatile semiconductor memory cells;

an error correction circuit making corrections on an error with respect to read/write data of the non-volatile semiconductor memory cells; and

a control circuit for controlling the non-volatile semiconductor memory cells,

wherein the interface, the error correction circuit and the control circuit include a first read mode booted via a first bootstrap to read data from the non-volatile semiconductor memory cells for continuously outputting (N + M)-byte (N is the n-th power of 2, n is positive integers, N > M) data via the interface, and a second read mode booted via a second bootstrap to read data from the non-volatile semiconductor memory cells for continuously outputting K-byte (K is the k-th power of 2, k is positive

integers) data via the interface after error corrections are made.

9. The device according to claim 8, wherein the first read mode is automatically transferred to an output standby state after continuously outputting the data, and the second read mode is automatically transferred to a normal operation mode after continuously outputting the data.

10. The device according to claim 8, wherein the plurality of non-volatile semiconductor memory cells have a ROM area storing system boot programs and an area except for the ROM area, and in the second read mode, K-byte (K > N) data is read from the ROM area.

11. The device according to claim 8, wherein the second read mode is booted according to a hardware reset signal supplied from an external device.

12. The device according to claim 8, wherein the second read mode is booted based on a software reset command from an external device.

13. The device according to claim 8, wherein during the second read mode, part of signals inputted to the interface is invalidated.

14. A non-volatile semiconductor memory device comprising:

a plurality of electrically data rewritable non-volatile semiconductor memory cells;

an interface making data exchange with an external

device to read/write data with respect to the non-volatile semiconductor memory cells;

an error correction circuit making corrections on an error with respect to read/write data of the non-volatile semiconductor memory cells; and

a control circuit for controlling the non-volatile semiconductor memory cells,

wherein the interface, the error correction circuit and the control circuit include a first write mode booted via a first bootstrap to receive (N + M)-byte (N is the n-th power of 2, n is positive integers, N > M) data inputted from the interface for collectively writing the data to the plurality of memory cells, and a second write mode booted via a second bootstrap to receive K-byte (K is the k-th power of 2, k is positive integers) data inputted from the interface to automatically generate a check code for error correction with respect to the K-byte data for collectively writing the K-byte data and the check code to the plurality of memory cells.

15. The device according to claim 14, wherein the interface, the error correction circuit and the control circuit further comprise:

a first read mode of reading data from the non-volatile semiconductor memory cells via a third bootstrap, and continuously outputting (N + M)-byte (N is the n-th power of 2, n is positive integers, N > M)

data via the interface; and

a second read mode of reading data from the non-volatile semiconductor memory cells via a fourth bootstrap, and continuously outputting K-byte (K is the k-th power of 2, k is positive integers) data via the interface after error corrections are made.

16. The device according to claim 15, wherein the first read mode is automatically transferred to an output standby state after continuously outputting the data, and the second read mode is automatically transferred to a normal operation mode after continuously outputting the data.

17. The device according to claim 15, wherein the plurality of non-volatile semiconductor memory cells have a ROM area storing system boot programs and an area except for the ROM area, and in the second read mode, K-byte (K > N) data is read from the ROM area.

18. The device according to claim 15, wherein the second read mode is booted according to a hardware reset signal supplied from an external device.

19. The device according to claim 15, wherein the second read mode is booted based on a software reset command supplied from an external device.

20. The device according to claim 15, wherein during the second read mode, part of signals inputted to the interface is invalidated.

21. A non-volatile semiconductor memory device

comprising:

a plurality of memory cell arrays each including a plurality of electrically data rewritable non-volatile semiconductor memory cells arranged in an array;

an interface making data exchange with an external device to write/read data with respect to the non-volatile semiconductor memory cells; and

a control circuit for controlling the non-volatile semiconductor memory cells,

wherein the interface and the control circuit include:

a first operation mode of making access with respect to one of the memory cell arrays via a first bootstrap to process (N + M)-byte (N is the n-th power of 2, n is positive integers, N > M) data; and

a second operation mode of making access with respect to at least two of the memory cell arrays via a second bootstrap to process K-byte (K is the k-th power of 2, k is positive integers) data.

22. A non-volatile semiconductor memory device comprising:

a plurality of electrically data rewritable non-volatile semiconductor memory cells;

an interface making data exchange with an external device to write/read data with respect to the non-volatile semiconductor memory cells;

a control circuit for controlling the non-volatile

semiconductor memory cells; and

a power supply voltage detection circuit detecting a power supply voltage, and outputting a boot signal to the control circuit,

wherein the interface and the control circuit include:

a first read mode for reading data from the non-volatile semiconductor memory cells via a first bootstrap booted by a signal inputted to the interface for continuously outputting data at the maximum of (N + M)-byte (N is the n-th power of 2, n is positive integers, N > M) via the interface; and

a second read mode for reading data from the non-volatile semiconductor memory cells via a second bootstrap booted by the boot signal, and continuously outputting data at the maximum of K-byte (K is the k-th power of 2, k is positive integers) via the interface.

23. The device according to claim 22, wherein the plurality of non-volatile semiconductor memory cells include an ROM area storing system boot programs and an area except for the ROM area, and in the second read mode data at the maximum of K-byte (K > N) is read from the ROM area.

24. The device according to claim 22, further comprising:

an error correction circuit, which corrects an error of the data read in the second read mode.

25. The device according to claim 22, wherein during the second read mode, part of signals inputted to the interface is invalidated.

26. A non-volatile semiconductor memory device comprising:

a plurality of electrically data rewritable non-volatile semiconductor memory cells;

an interface making data exchange with an external device to write/read data with respect to the non-volatile semiconductor memory cells;

a control circuit for controlling the non-volatile semiconductor memory cells;

a power supply voltage detection circuit detecting a power supply voltage, and outputting a boot signal to the control circuit; and

an error correction circuit,

wherein the interface and control circuit include:

a first read mode booted by a signal inputted to the interface to read data from the non-volatile semiconductor memory cells;

a second read mode booted by the boot signal to read the data from the non-volatile semiconductor memory cells so as to make corrections on the data by the error correction circuit.

27. The device according to claim 26, wherein the plurality of non-volatile semiconductor memory cells include an ROM area storing system boot programs and

an area except for the ROM area, and data is read from the ROM area in the second read mode.

28. The device according to claim 26, wherein during the second read mode, part of signals inputted to the interface is invalidated.

29. An electronic card loaded with the non-volatile semiconductor memory device described in claim 1.

30. An electronic card loaded with the non-volatile semiconductor memory device described in claim 8.

31. An electronic card loaded with the non-volatile semiconductor memory device described in claim 14.

32. An electronic card loaded with the non-volatile semiconductor memory device described in claim 21.

33. An electronic card loaded with the non-volatile semiconductor memory device described in claim 22.

34. An electronic card loaded with the non-volatile semiconductor memory device described in claim 26.

35. An electronic apparatus comprising:

the electronic card described in any one of claims 29 to 34;

a card slot electrically connectable to the

electronic card; and

a card interface connected to the card slot.

36. The apparatus according to claim 35, wherein the electronic apparatus is a digital still camera.

37. The apparatus according to claim 35, wherein the electronic apparatus is a personal digital assistant.

38. The apparatus according to claim 35, wherein the electronic apparatus is a voice recorder.

39. The apparatus according to claim 35, wherein the electronic apparatus is a PC card.

40. An electronic apparatus comprising:

a non-volatile semiconductor memory device including a plurality of electrically data rewritable non-volatile semiconductor memory cells, an interface making data exchange with an external device to write/read data with respect to the non-volatile semiconductor memory cells, and a control circuit for controlling the non-volatile semiconductor memory cells; and

a controller for controlling the non-volatile semiconductor memory device,

wherein the interface and the control circuit include:

a first read mode for reading data from the non-volatile semiconductor memory cells via a first bootstrap, and continuously outputting the data at the

maximum of (N + M)-byte (N is the n-th power of 2, n is positive integers, N > M) via the interface; and

a second read mode for reading the data from the non-volatile semiconductor memory cells via a second bootstrap, and continuously outputting the data at the maximum of K-byte (K is the k-th power of 2, k is positive integers, K > N) via the interface, and

wherein the data read in the second read mode is a program for booting the electronic apparatus.

41. The apparatus according to claim 40, wherein the non-volatile semiconductor memory device further includes an error correction circuit to correct an error of the data read in the second read mode.

42. The apparatus according to claim 40, wherein the non-volatile semiconductor memory device further includes a power supply voltage detection circuit to detect a power supply voltage and outputs a boot signal to the control circuit, the first read mode is booted by a signal inputted to the interface, and the second read mode is booted by the boot signal.

43. The apparatus according to claim 40, wherein, during the second read mode, part of signals inputted to the interface is invalidated.

44. The apparatus according to claim 40, which further comprises an SRAM.

45. An electronic apparatus comprising:

a non-volatile semiconductor memory device

including a plurality of non-volatile semiconductor memory cells electrically data rewritable, an interface making data exchange with an external device to write/read data with respect to the non-volatile semiconductor memory cells, a control circuit for controlling the non-volatile semiconductor memory cells, and an error correction circuit; and

a controller for controlling the non-volatile semiconductor memory device,

wherein the interface and the control circuit include:

a first read mode for reading data from the non-volatile semiconductor memory cells via a first bootstrap; and

a second read mode for reading the data from the non-volatile semiconductor memory cells via a second bootstrap so as to correct an error of the data read by the error correction circuit,

and wherein the data read in the second read mode is a program for booting the electronic apparatus.

46. The apparatus according to claim 45, wherein the non-volatile semiconductor memory device further includes a power supply voltage detection circuit for detecting a power supply voltage to output a boot signal to the control circuit, the first read mode is booted by a signal inputted to the interface, and the second read mode is booted by the boot signal.

47. The apparatus according to claim 45, wherein during the second read mode, part of signals inputted to the interface is invalidated.

48. The apparatus according to claim 45, which further comprises an SRAM.

49. An electronic apparatus comprising:

a non-volatile semiconductor memory device including a plurality of electrically data rewritable non-volatile semiconductor memory cells, an interface making data exchange with an external device to write/read data with respect to non-volatile semiconductor memory cells, and a control circuit for controlling the non-volatile semiconductor memory cells; and

a controller for controlling the non-volatile semiconductor memory device,

wherein the interface and the control circuit include:

a first read mode for reading data from the non-volatile semiconductor memory cells via a first bootstrap; and

a second read mode for reading the data from the non-volatile semiconductor memory cells via a second bootstrap,

and wherein part of signals inputted to the interface is invalidated during the second read mode, and data read in the second read mode is a program for

booting the electronic apparatus.

50. The apparatus according to claim 49, wherein the non-volatile semiconductor memory device further includes an error correction circuit to correct an error of the data read in the second read mode.

51. The apparatus according to claim 49, wherein the non-volatile semiconductor memory device further includes a power supply voltage detection circuit, which detects a power supply voltage and outputs a boot signal to the control circuit, the first read mode is booted by a signal inputted to the interface, and the second read mode is booted by the boot signal.